

REMARKS

In the parent application Ser. No. 09/768,580 filed January 23, 2001, a non-final Office Action dated October 23, 2002 rejected claims 21-27 under 35 U.S.C. § 112 and 35 U.S.C. § 103(a). Claims 21-27 having been canceled. However, new claims 28-40 have been added. Therefore, the Applicant will address the rejections from the parent application to the extent that they may apply to new claims 28-40.

Support for the new claims can be found in the Detailed Description section of the current application at page 18-23 and at page 14, lines 1-5. No new subject matter has been added with these amendments.

A. 35 U.S.C. § 112

Claims 21-27 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 21-27 have been canceled. Therefore, reconsideration and withdrawal of the rejection is respectfully requested.

B. 35 U.S.C. § 103(a)

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based

on applicant's disclosure. *In re Vaack*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Hsu in view of Ueda - Claims 21, 26, and 27

Claims 21, 26, and 27 of the parent application stand rejected under 35 U.S.C. § 103(a) as being obvious over the U.S. Patent No. 5,633, 530 issued May 27, 1997 to Chen Chung Hsu (hereinafter "the Hsu patent") (Office Action, page 4) in view of the U.S. Patent No. 5,701,033 issued December 23, 1997 to Tetsuya Ueda, et al. (hereinafter "the Ueda patent") (Office Action, page 4).

As previously discussed, claims 21, 26, and 27 have been canceled. Thus, the present rejection is moot. However, to the extent that the Hsu patent and the Ueda patent may apply to new claims 28-40, new independent claim 28 (from which claims 29-40 depend) contains a limitation of a flip-chip attached to a ceramic substrate. The Hsu patent does not teach or suggest a flip-chip being electrically connected to a ceramic substrate. In fact, the Hsu patent teaches away from electrically connecting a flip-chip to a ceramic substrate, since the substrate 16 of Hsu is simply a covering plate, and is not electrically connected to the chip (col 3, lines 15-16). Neither does the Ueda patent teach or suggest a flip-chip being electrically connected to a ceramic substrate, since the capacitor chip of Ueda is mounted to a lowered step surface, and does not electrically connect with the capacitor in the same manner as a connection to a flip-chip, i.e. through solder balls (col. 3, lines 60-63). Thus, the Hsu patent and the Ueda patent, either alone or in combination, neither teaches or suggests electrically connecting a flip-chip to a ceramic substrate.

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"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In *re Royka*, 490 F.2d 981,180 USPQ 580 (CCPA 1974). Because the Hsu patent and the Ueda patent, either alone or in combination, do not teach or suggest all of the claim limitations of claims 28-38, they are not rendered obvious by the Hsu patent in view of the Ueda patent.

Hsu in view of Chia - Claims 22 and 23

Claims 22 and 23 of the parent application stand rejected under 35 U.S.C. § 103(a) as being obvious over the Hsu patent in view of the U.S. Patent No. 5,563,446 issued October 8, 1996 to Chok J. Chia, et al. (hereinafter "the Chia patent") (Office Action, page 5).

As previously discussed, claims 22 and 23 have been canceled. Thus, the present rejection is moot. However, to the extent that the Hsu patent and the Chia patent may apply to new claims 28-40, new independent claim 28 (from which claims 29-40 depend) contains a limitation of a flip-chip attached to a ceramic substrate. As previously discussed, the Hsu patent does not teach or suggest a flip-chip being electrically connected to a ceramic substrate. Furthermore, the Chia patent does not overcome this void in the teaching of the Hsu patent, as the Office relies on the Chia patent for a teaching of filling the package above a chip with an encapsulant.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In *re Royka*, 490 F.2d 981,180 USPQ 580 (CCPA 1974). Because the Hsu patent and the Chia patent, either alone or in combination, do

not teach or suggest all of the claim limitations of claims 28-40, they are not rendered obvious by the Hsu patent in view of the Chia patent.

Hsu in view of Wenzel - Claims 24 and 25

Claims 24 and 25 of the parent application stand rejected under 35 U.S.C. § 103(a) as being obvious over the Hsu patent in view of the U.S. Patent No. 5,633,530 issued November 21, 2000 to James F. Wenzel, et al. (hereinafter "the Wenzel patent") (Office Action, page 5).

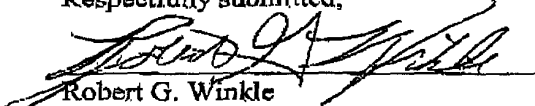
As previously discussed, claims 24 and 25 have been canceled. Thus, the present rejection is moot. However, to the extent that the Hsu patent and the Chia patent may apply to new claims 28-40, new independent claim 28 (from which claims 29-40 depend) contains a limitation of a flip-chip attached to a ceramic substrate. As previously discussed, the Hsu patent does not teach or suggest a flip-chip being electrically connected to a ceramic substrate. Furthermore, the Wenzel patent does not overcome this void in the teaching of the Hsu patent, as the Office relies on the Wenzel patent for a teaching of a chip that can be a CPU, SDRAM, etc.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In *re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Because the Hsu patent and the Wenzel patent, either alone or in combination, do not teach or suggest all of the claim limitations of claims 28-40, they are not rendered obvious by the Hsu patent in view of the Wenzel patent.

In view of the foregoing remarks, the Applicants request allowance of the application. Please forward further communications to the address of record. If the Examiner needs to contact the below-signed attorney to further the prosecution of the application, the contact number is (208) 133 9217.

Respectfully submitted,

Dated: April 25, 2003

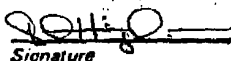

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VERSION OF CLAIMS WITH MARKINGS

IN THE CLAIMS:

21. (Canceled) A method of constructing a multi-chip package, comprising:
placing a first chip package on a first shelf;
electrically attaching said first chip package to a plurality of shelves with direct connections between said first chip package and said plurality of shelves;
placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and
electrically attaching said second chip package to said second shelf with direct connections between said second chip package and said second shelf.
22. (Canceled) The method of claim 21 further comprising the step of filling said multi-chip package above said second chip package with an encapsulant.
23. (Canceled) The method of claim 22 wherein said step of placing said second chip package on said second shelf further comprises placing said second chip package on said second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip.
24. (Canceled) The method of claim 21 wherein said step of placing a first chip package further comprises placing a CPU chip package on a first shelf.
25. (Canceled) The method of claim 21 wherein said step of placing said second chip

package further comprises placing a memory cache on a second shelf.

26. (Canceled) The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said plurality of shelves.

27. (Canceled) The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said plurality of shelves.

28. (New) A method of constructing a multi-chip package, comprising:
electrically connecting a semiconductor die to at least one of a plurality of shelves;
electrically connecting a flip-chip to a ceramic substrate; and
attaching said ceramic substrate to one of said plurality of shelves.

29. (New) The method of claim 28, further comprising electrically connecting said ceramic substrate to at least one of said plurality of shelves.

30. (New) The method of claim 29, wherein electrically connecting said ceramic substrate to at least one of said plurality of shelves comprises electrically connecting said ceramic substrate to at least one of said plurality of shelves with at least one bond wire.

31. (New) The method of claim 28, wherein attaching said ceramic substrate to one of said plurality of shelves provides a lid above said semiconductor die.

32. (New) The method of claim 28, further comprising electrically testing said electrically connected flip-chip before attaching said ceramic substrate to said one of said plurality of shelves.

33. (New) The method of claim 28, wherein electrically connecting said flip-chip to said ceramic substrate comprises electrically connecting said flip-chip to said ceramic substrate with solder balls.

34. (New) The method of claim 28, further comprising covering said flip-chip with an encapsulant.

35. (New) The method of claim 28, further comprising disposing a seal between a base of said ceramic substrate and said one of said plurality of shelves to which said ceramic substrate is attached.

36. (New) The method of claim 28, wherein electrically connecting said semiconductor die to said at least one of a plurality of shelves comprises electrically connecting a CPU chip to said at least one of said plurality of shelves.

37. (New) The method of claim 28, wherein electrically connecting said flip-chip to said ceramic substrate comprises electrically connecting a memory cache flip-chip to said ceramic substrate.

38. (New) The method of claim 28, wherein electrically connecting said semiconductor die to at least one of said plurality of shelves comprises electrically connecting said semiconductor die to said at least one of a plurality of shelves with at least one bond wire.

39. (New) The method of claim 28, further including attaching said semiconductor die to a slug.

40. (New) The method of claim 39, further comprising attaching said slug to at least one of a plurality of shelves.